REMARKS

Favorable reconsideration of this application is respectfully requested.

The present invention relates to a storage switch for use in storage area networks (SANs) that afford high bandwidth and substantially improved performance and simplicity over conventional storage switches and switching systems. Storage switch architectures and methods in accordance with the invention enable multi-protocol SANs that are capable of processing data packets for virtualization and translation between storage protocols at "wire speed", i.e., at the incoming speed of the packet at an associated switch port without introducing any more latency than would be introduced by a switch that merely performed switching or routing functions. This affords switches that process data packets on-the-fly without buffering the data packets as is done in conventional switches. Thus, compared with conventional practices, switch architectures and methods in accordance with the invention minimize the time required to process packets, and have a higher throughput rate than conventional switches.

The significant advantages afforded by the invention and which distinguish the claimed invention from conventional SANs are due, in part, to the fact that the storage switches in accordance with the invention which connect a plurality of distributed hosts or servers with a plurality of distributed storage devices distribute intelligence to every switch port. This enables simplified centralized management of globally distributed storage devices. The storage switches integrate many of the various functions

previously performed in a SAN by discrete elements, such as an appliance and gateway, into a unified storage switch. Intelligent switches in accordance with the invention perform not only traditional switching functions, they also provide virtualization and storage services, such as mirroring, as well as protocol translation to integrate different storage protocols into a unified network (see specification, pages 12-13, paragraph [0060]).

Furthermore, the distributed intelligence afforded by the invention allows a switch to process packets at "wire speed" and "without buffering", i.e., without introducing any more latency that would be introduced by a switch that merely performs switching or routing functions (see specification, page 6, paragraph [0015], lines 15-22; and page 13, paragraph [0062], lines 12-15.) In particular, as used in the specification (see page 13, paragraph [0062], lines 15-16), the term "wire speed" is defined to be a speed measured by the connection to the particular switch port. Thus, the term "wire speed" means that a storage switch can handle the maximum packet throughput rate for the type of connection to that switch port. For example, as described on page 13 of the specification, if the connection to a port is an OC-48 connection (2.5 bits per nsec), wire speed means that the switch must keep up with that data rate. Similarly, if a switch port is 1 Gb Ethernet, wire speed processing will be 1 bit per nsec; and if the port is 2 Gb Fibre Channel the wire speed will be 5 μsec per Kilobyte, etc. In order to process packets at wire speed, a storage switch in accordance with the invention will not buffer packets, as done in conventional switches, but rather processes the packets on-the-fly (see specification, page 18, paragraph [0078]; page 33, paragraph [0127]). Intelligent switches in accordance with

the invention have an architecture that minimizes the processing time for packets and avoids buffering to enable wire speed to be met.

I. The Distinguishing Elements

The various rejections of the claims under 35 U.S.C. §102(e) and §103(a) are respectfully traversed. For the reasons which follow, it is respectfully submitted that the prior art of record can neither anticipate nor render obvious Claims 1-6 and 8-45, and that these claims are allowable over the cited prior art.

This application contains eight independent claims. These are independent Claims 1, 15, 20 and 24 directed to a switch for use in a network, independent Claims 21 and 35 directed to a storage network, and independent Claims 42 and 43 directed to a method for use by a device in a system for storing and accessing data. All independent claims of this application, as well as a number of the dependent claims, recite either one of two different claim elements (limitations) which are neither disclosed nor suggested by the cited prior art. Thus, either of these two elements distinguishes the claims over the cited prior art and renders the claims patentable.

As will be explained more fully below, these two different distinguishing claim elements are:

(i) that the claimed switch, network or method processes packets "without buffering the packet", and

(ii) that the switch or method processes packets "at wire speed".

The independent claims that recite either one of these two elements (as well as several dependent claims), and the claims which depend from the independent claims, are allowable over the prior art of record for at least their recitation of one of these distinguishing elements. Moreover, the claims are also allowable over the cited prior art for other recitations, as will be discussed more fully below. For the reasons set forth below, it is respectfully submitted that none of the claims is either anticipated or rendered obvious by the cited prior art references, considered either individually or in combination.

First, the claims which recite either one of the two distinguishing elements "without buffering" and "at wire speed" will be discussed and distinguished from the cited prior art. Next, other distinguishing limitations of these claims, as well as the rejections of other claims will be addressed.

A. Without Buffering

Independent Claims 1, 15, 24, and 43, as well as dependent Claims 9 and 27 all explicitly recite that packets are processed "without buffering". None of the prior art references cited discloses or suggests a switch, a storage network or a method as claimed, where packets are processed "without buffering". In fact, the primary references relied upon by the Office teach just the opposite.

U.S. Patent No. 6,438,595 to Blumenau, a primary reference relied upon in support of the rejection under 35 U.S.C. §102(e), discloses a cached storage subsystem which comprises a storage controller having a cache memory that

connects storage volumes (devices) to a data network (see Figure 1). As described at column 4, lines 37-54, when a port adapter receives a storage access request from a host of the data network, the port adapter accesses a directory in the cache memory to determine whether the data resides in the cache memory. If the data to be accessed resides in the cache memory, then the port adapter accesses the data in the cache memory (col. 4, lines 41-43). If it does not, one of the storage adapters determines where in a storage device the data resides, reads the data from the appropriate storage device, and writes the data to the cache memory (see col. 4, lines 44-51) (emphasis added) . The storage adapters also perform a write-back operation to insure that data written to the cache memory by the port adapters eventually is written to the storage volumes (col. 4, lines 51-54)(emphasis added). This is a clear disclosure of data being written to and read from the storage devices by first writing and reading the data to cache memory, i.e., buffering of data. Thus, Blumenau '595 expressly teaches away from the claimed element of processing data "without buffering".

A second primary reference relied upon by the Office, and which is asserted to show processing without buffering, is published application US 2002-0004883 to Nguyen et al. The Office wrongly asserts (see paragraph 15, page 6 of the Office Action) that there is no buffering done at the switch side, and there is no store and forward at the switch in Nguyen. It is respectfully submitted that this is an incorrect characterization of Nguyen.

To begin with, Nguyen et al. discloses a network attached storage system, rather than a SAN system, comprising a data network having data processors (DP1-4) and storage devices (TD1-5) connected to a data network ("N") by connection blocks (CB1-9). There are no storage switches, as claimed, disclosed in Nguyen. The connection blocks perform a translation between physical and virtual addresses. (See Figure 4 and paragraph [0027], second column.) The network additionally includes a tape system controller comprising another data processor (ASCS) and another connection block (CB0). As explained in Nguyen with respect to Figure 5, during a data transfer operation where data is transferred from a data processor to a connection block, the connection block ". . . will buffer the data and transfer it to the physical tape devices TD 1, TD 2, TD 3 via CB 5, CB 6, and CB 7." (Emphasis added) (See paragraph [0029], page 4). This is an explicit disclosure of buffering packets that are being processed, and is contrary to the Office's assertion of a disclosure of "without buffering". Accordingly, the reference cannot anticipate (or render obvious) the claims that recite that processing occurs without buffering.

Another principal reference relied upon by the Office for purportedly showing processing data without buffering is U.S. Patent No. 6,260,120 to Blumenau et al. The disclosure of the Blumenau '120 patent is similar to that of Blumenau '595. Blumenau '120 discloses a substantially similar cache storage subsystem to Blumenau '595 that transfers data between storage devices and a network by writing and reading data to and from storage devices first via the cache memory, i.e., a buffer, for access by a port adapter, as previously described above. Like Blumenau '595, it performs a write-back operation to insure that data written to the cache memory by the port adapters

eventually becomes written to the storage volumes (see Blumenau '120 column 8, lines 55-65).

Contrary to the Office's assertion, there is nothing in Blumenau '120 at columns 25 or 26 that discloses or suggests that data processing may be "without buffering". At column 25, lines 18-27 and at column 26, lines 1-25, Blumenau '120 discusses the operation of hosts and port adapters with the cache storage system. There is no disclosure or suggestion in these locations of processing packets without buffering. Also, at column 26, lines 25-65, the reference describes mapping of information between storage volumes and virtual ports to create a virtual port mapping table and optional lists 283 which may be used for storage access by a host. This also has nothing to do with the optional processing of packets without buffering, as asserted by the Office (Office Action, page 19, paragraph (g)). There is no disclosure in the reference of processing of packets without buffering, as claimed.

Accordingly, none of the primary prior art references relied upon by the Office, and none of the secondary references, discloses or suggests processing packets without buffering, as set forth in independent Claims 1, 15, 24 and 43, or in dependent Claims 9 and 27. Accordingly, none of the cited references can anticipate these claims, and there is no teaching or suggestion in any of the references which would render these claims obvious.

B. At Wire Speed

As to the second distinguishing element of the claims, independent Claims 20, 21, 35 and 42, and dependent Claims 8, 10, 28 and 44 all explicitly recite that packets are processed "at wire speed".

As discussed above, the specification defines wire speed relative to the speed of the connection to the particular port of the switch on which packets are sent or received. The specification states that packets processed "at wire speed" incur no more latency than would be introduced by a switch merely performing switching or routing functions, and that to process data at wire speed means that the invention does not buffer packets as is done conventionally.

None of the cited prior art references discloses or suggests processing packets at wire speed, as claimed. Accordingly, none of the cited references can either anticipate or render obvious any of independent Claims 20, 21, 35 and 42 (or any of the claims dependent thereon), and none can anticipate or render obvious dependent Claims 8, 10, 28 and 44 which recite this limitation.

Contrary to the Office's assertion, Blumenau '595 does not disclose (or suggest) in Figures 1-3, or at column 5, lines 25-30, processing packets at wire speed. Rather, Blumenau discloses at column 5, lines 12-24 the operation of the port adapters and storage adapters using programmed microprocessors for handling the communication protocol of storage devices and communicating with the cache memory; and at lines 25-30, Blumenau discloses examples of links between the storage adapters and

storage devices as being FWD SCSI or Fibre Channel fiber-optic loops. This disclosure merely describes the types of storage protocols used, but says nothing with regard to the processing of packets at wire speed.

In connection with the rejection of Claim 21 the Office asserts (see Office Action, page 5, paragraph 13) that Blumenau at Column 5, lines 13-31 discloses performing processing at wire speed because, as asserted by the Office, ". . . wire speed here is in accordance with the line speed of the network". Nothing in the reference relates to or discloses processing packets at wire speed. Network speed has nothing to do with wire speed as that term is defined in the specification and used in the claims. As previously noted, wire speed is defined as the speed of the connection to a particular port at which packets are received or sent; and "processing" refers to packets entering that port being processed for, e.g., virtualization or translation, without buffering. There is no disclosure or suggestion of this in Blumenau '595.

The disclosure of Blumenau '120 is similar to Blumenau '595, as noted, and likewise contains no disclosure or suggestion of processing packets at wire speed. The Office's reference to Blumenau '120 as disclosing processing at wire speed (at Figures 1-4, 7, 21-30 and column 24, lines 56-67 and columns 25 and 26) mischaracterizes the reference. The reference does not disclose processing anything at wire speed, as claimed. At column 24, Blumenau '120 describes the Fibre Channel protocol for accessing storage volumes, but is silent at to any processing at wire

speed, contrary to the assertion by the Office. Additionally, as pointed out above, columns 25 and 26 have no disclosure at all relative to processing at wire speed.

As previously described, Nguyen at paragraph [0027] discloses nothing with respect to processing packets at wire speed, as asserted by the Office. In fact, as pointed out above, in paragraph [0029] Nguyen expressly discloses the buffering of data by the connection blocks upon transferring data to the physical tape drives. Also, in paragraph [0027], left column, Nguyen's reference to providing a requested data rate indicates that the requested data rate is achieved by ". . . striping the data requested coming from DP1 across devices TD1+TD2+. . . TD5", i.e., by writing the data in parallel to multiple drives. This has nothing to do with processing packets at wire speed, as claimed, and Nguyen cannot support a rejection of claims reciting this limitation.

Accordingly, in view of the foregoing, it is clear that none of the cited prior art discloses or suggests processing at wire speed, and cannot anticipate or render obvious any of independent Claims 20, 21, 35 and 42 or dependent Claims 8, 10, 28 and 44, or any of the dependent claims which depend from the independent claims reciting the wire speed element. Accordingly, these claims are allowable over the prior art for at least these reasons.

II. The Rejection of Claims 1, 4, 5, 8, 15, 18 and 21 under 35 U.S.C. §102(e)

The rejection of Claims 1, 4, 5, 8, 15, 18 and 21 as anticipated by Blumenau '595 is traversed. Independent Claim 1 has been amended to incorporate Claim 7 and

to recite that packets are processed "without buffering". Independent Claim 15 has similarly been amended to recite that packets are processed without buffering; and independent Claim 21 calls for a switch with means associated with each port for performing "wire speed" processing of packets. These independent claims and the claims which depend therefrom cannot be anticipated by Blumenau '595 since the reference discloses neither the "without buffering" nor the "wire speed" limitations, for the reasons discussed above. Accordingly, these claims are deemed to be allowable over the reference.

In addition to the reasons discussed above, independent Claims 1, 15 and 21 distinguish over Blumenau for other reasons. All are directed to a switch for use in a network, and the claims set forth the elements of the switch and the functions the elements perform. Claim 1 calls for the switch to comprise a plurality of line cards, each line card including a plurality of ports and a plurality of storage protocol processing units. Claim 15 is similar in calling for a plurality of processing units; and Claim 21 calls for the line card to have at least one port, and "means associated with the port for performing wire speed processing of packets". Blumenau does not disclose a switch for use in a network comprising those elements. Blumenau discloses a data network having a cached storage subsystem, as illustrated in Figure 1. The discrete components of the network do not constitute a switch, as claimed.

Although Blumenau does disclose that the data network has a port switch (see Figure 2) that switch does not have a plurality of line cards nor does it have a plurality of processing units associated with ports. Rather, as described in column 5, lines 37-

47, the switch performs merely a switching function to permit hosts to access any of the storage ports; and discloses (in column 6, lines 10-18) that the switch includes a control computer which is programmed to provide directory services. Claim 1 calls for the processing units to perform storage command processing for commands received at a port; and Claim 21 calls for means for performing wire speed processing of packets. None of these functions are performed by the port switch 32 of Blumenau. Rather, the portion of Blumenau cited by the Office in its rejection comprises the storage controller illustrated in Figure 1 of the cache storage subsystem. The storage controller does not constitute a switch as claimed.

In view of the foregoing, it is respectfully submitted that Blumenau '595 cannot anticipate Claims 1, 4, 5, 8, 15, 18 and 21.

III. The Rejection of Claims 20, 35 and 40-42 Under 35 U.S.C. §102(e)

The rejection of Claims 20, 35 and 40-42 as anticipated by Nguyen et al. is respectfully traversed. Independent Claims 20, 35 and 42 all call for processing of packets "at wire speed", and cannot be anticipated by Nguyen since Nguyen has no such disclosure, for the reasons discussed above.

Moreover, Claim 20 calls for each processing unit associated with a port to include a classifier. As defined in the specification (see page 28, paragraph [0113]), the term "classification" refers to classifying packets as either data packets or control packets. A "classifier" is an element that performs the classification function. Nguyen does not include a packet classifier, and does not otherwise perform a packet

classification function. As described above, Nguyen discloses a network (N) having attached storage systems and data processors connected to the network by connection blocks CB1-CB9. The connection blocks perform "translation" to convert between physical and vertical addresses. They do not perform classification. This is because classification is unnecessary. The network "N" of Nguyen is a data network that only carries data. Nguyen disclosed a second control network "CN" that is separate from the data network N. Control commands from the data processors are carried on the separate control network "CN" (see specification, paragraph [0007] and [0027]). Accordingly, Nguyen does not need to perform a packet classification function as recited in Claim 21, and discloses nothing about classification. Therefore, Nguyen cannot anticipate the claim for this reason also.

As to independent Claim 35, contrary to the Office's assertion Nguyen does not disclose a switch. The combination of DP1 and CB1-CB4 does not constitute a switch, as claimed. These are separate elements of Nguyen consisting of a data processor and connection blocks. These separate elements cannot be grouped as proposed to form a switch, as claimed. Moreover, Nguyen does not disclose processing packets at wire speed as explained above, and cannot anticipate Claim 35 for this reasons alone.

Claim 42 further calls for determining whether a packet is a data packet or control packet, forwarding a control packet to a central processing unit, and sending the packet to a physical target formatted in accordance with another storage protocol at wire speed if the packet is a data packet. Nguyen does not either classify or handle packets as data packets and control packets, as claimed. Accordingly, Nguyen cannot

anticipate Claim 42 for at least this reason. Furthermore, Claim 42 recites processing packets at wire speed. Nguyen does not disclose processing data packets at wire speed, as pointed out above, and also cannot anticipate Claim 42 for this reason.

Claims 40 and 41 depend from Claim 35 and cannot be anticipated by Nguyen for the same reasons Claim 35 cannot be anticipated.

IV. The Rejections Under 35 U.S.C. §103(a)

The various rejections of the remaining claims under 35 U.S.C. §103(a) is based upon a combination of either Blumenau '595 or Nguyen and combinations of various ones of the secondary references. These rejections are all traversed. None of the prior art of record, either alone or in combination, teaches or suggests the recitations of any of the independent claims or of the claims dependent thereon, and cannot render these claims obvious.

A. The Rejection of Claims 7, 9-14, 16-17, 24-29, 32, 34, 43 and 44

The rejection of these claims under 35 U.S.C. §103(a) based upon Blumenau '595 in combination with Blumenau '120 is traversed.

Independent Claim 24 has been amended to recite that the processing of data packets received at a port is performed "without buffering", and independent Claim 43 sets forth a method where all the steps of the method are performed "without buffering". For the reasons pointed out above, neither Blumenau '595 nor Blumenau '120 discloses or suggests processing packets without buffering. In fact, as pointed

out above, both references explicitly teach that data written to or read from the storage devices is written or read via the cache memory 32 of the cached storage subsystem, i.e., the packets are buffered. Therefore, neither of these two references, alone or in combination, can teach or suggest Claim 24, or Claims 25-34 which depend therefrom, or Claim 43 and dependent Claim 44. Accordingly, these claims are deemed allowable over the two Blumenau references.

The remaining secondary references cited by the Office do not cure the deficiencies of the two Blumenau references or of Nguyen, and these secondary references cannot alone or in combination with the Blumenau references or Nguyen render any of the dependent claims obvious.

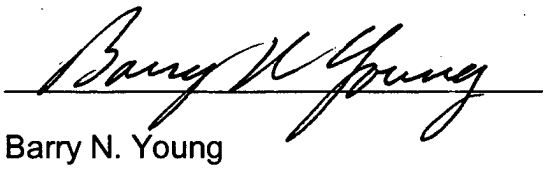
In view of the foregoing, it is respectfully submitted that the rejections of the claims under 35 U.S.C. §102(e) and under 35 U.S.C. §103(a) are improper and should be withdrawn, and that Claims 1-6 and 8-44 are allowable. Accordingly, favorable reconsideration of this application is respectfully requested and early allowance of all claims is solicited.

The specification has been amended to update the status of the applications referred to on page 1 - 2.

If upon consideration of this Amendment any outstanding issues remain, it is requested that the examiner contact the undersigned before taking further action.

Dated: March 8, 2006

Respectfully Submitted,



Barry N. Young
Attorney for Assignee
Reg. No. 27,744

Customer No. 48789
Law Offices of Barry N. Young
Court House Plaza, Suite 410
260 Sheridan Avenue
Palo Alto, CA 94306-2047
Phone: (650) 326-2701
Fax: (650) 326-2799
byoung@young-iplaw.com